

## Features and Benefits

- Supply voltage up to 12 V.
- Interface directly with 3.3/5 V CMOS logic  $\mu$ P
- Serial peripheral interface
- Can drive two air core actuators over the full 360° and one over 90°.
- Open circuit or short circuit detection of the drivers' outputs.
- Small size (SSOP20 package)
- Real time angle tracking

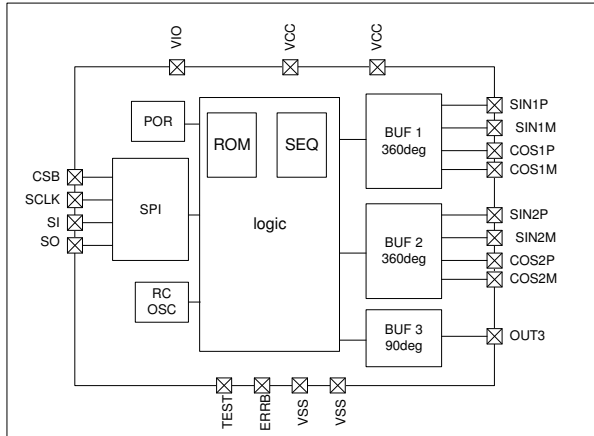
## Applications

- Air-core meter Driver Dashboard
- Industrial Metering

## Ordering Information

Part No.	Temperature Code	Package Code	Option code
MLX10420	R (-40 to 105°C)	FR20 (SSOP20 209mil)	

### 1 Functional diagram



### 2 General Description

The MLX10420 is a  $\mu$ P peripheral for air-core meters control using SIN/COS PWM commands. The circuit controls two independent sets of CMOS power bridges. A ten bit angle is displayed with 9 bits per quadrant. The PWM frequency is set by an on chip oscillator. A power-on self test detects open or short-circuits outputs for each air-core meter and a real time angle tracking avoids display errors.

The chip can also drive one small angle air-core meters (90°).

The communication with the  $\mu$ P is done via a three wires serial link.

The chip outputs an error status on a special pin.

### 3 History

Table 1 shows the revisions of this document.

Version	Date	Name	Description
1.0	20/4/07	hva	Initial version
1.1	2/8/07	hva	Major rework
1.2	3/10/07	hva	Rework at DI phase
1.3	02/06/08	fbe	Updated SPI message format
1.4	09/10/08	fbe	Updated block diagram (missing VIO pin) §6 Updated Calibration procedure timings from 16us to 17.5us §12.4.5.4
1.5	13/05/2009	fbe	Layout rework

Table 1: revision history

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## 7 Glossary of Terms

Table 2 explains the abbreviations used in this document.

CMOS	Complementary Metal Oxide Semiconductor (standard logic family)
DC	direct current
ESD	Electro-Static Discharge
HBM	human body model (for ESD)
i.e.	'id est' ... which is ...
POR	Power On Reset
PWM	Pulse Width Modulation
RCOSC	RC oscillator
rev	revision
RT	room temperature
TA	ambient temperature
TC	temperature coefficient
tri-state	high impedant state of a driver output

Table 2: abbreviations used in this document

## 8 Maximum ratings

Table 3 shows the maximum ratings of the chip.

Parameter.	Min	Max	Unit
<b>Supply</b>			
Supply voltage range VCC	-0.3	14	V
maximum supply current at VCC		100	mA
Supply voltage range VIO	-0.3	5.5	V
maximum supply current at VIO		3	mA
<b>Others</b>			
Operating ambient Temperature Range, $T_A$	-40	105	°C
Storage Temperature Range, $T_S$	-50	150	°C
ESD Sensitivity (AEC Q100 002), equivalent to discharge 100pF with 1.5kOhms	-2	2	kV
Maximum continuous current in motor driver	--50	50	mA

Table 3: absolute maximum ratings

Exceeding the absolute maximum ratings in Table 3 may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note:

- *Latch-up immunity will be verified according to AEC Q100 004.*
- *the maximum ratings are valid over the full operating temperature range,  $T_A$*

## 9 Pad definitions and descriptions

Pin	Pad Name	Function
1	VCC	Supply
2	SIN1P	Output buffer (coil 1 air-core 1 )
3	SIN1M	Output buffer (coil 1 air-core 1 )
4	VSS	Ground
5	COS1P	Output buffer (coil 2 air-core 1 )
6	COS1M	Output buffer (coil 2 air-core 1 )
7	OUT3	Output buffer (air-core 3 )
8	VCC	Supply
9	ERRB	Error output
10	TEST	Input
11	SI	Serial Data IN
12	SCLK	Serial clock
13	VIO	Supply for the digital interface pins
14	CSB	Chip select
15	SO	Serial Data OUT
16	COS2M	Output buffer (coil 2 air-core 2 )
17	COS2P	Output buffer (coil 2 air-core 2 )
18	VSS	Ground
19	SIN2M	Output buffer (coil 1 air-core 2 )
20	SIN2P	Output buffer (coil 1 air-core 2 )

Table 4: Pinout of MLX10420

Pin-out diagram:

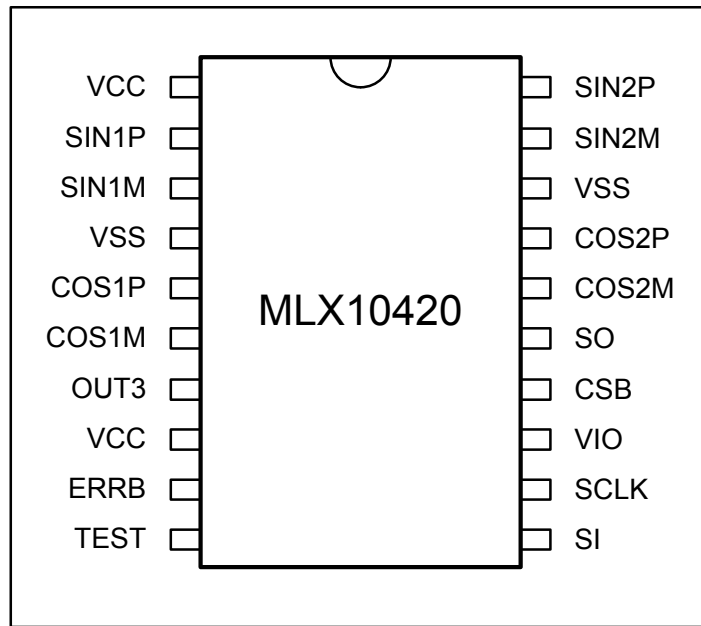


Figure 1: Pinning diagram

SSOP20 Package information Table 5 gives the information that will be available on the top side of the package.

X	CHIP VERSION
NNNNNNN	LOT NUMBER
YY	YEAR CODE
WW	WEEK CODE

Table 5: SSOP20 package information

## 10 General Electrical Specifications

### 10.1 Static Characteristics

The static characteristics are shown in Table 6. The device works up to specification from -40°C till 105°C, VCC = 4.5V to 12V, unless otherwise specified. Positive currents flow into the IC.

Parameter.	Symbol	Test Conditions	Min	Typ	Max	Units
<b>VCC supply</b>						
Supply current	ICC	Inputs at VCC or VSS, no loads on outputs			5.5	mA
Maximum power dissipation	PDmax				200	mW
<b>VIO supply</b>						
Supply voltage (note 2)	VIO		3		5.5	V
Supply current	IIO	Inputs at VCC or VSS, no loads on outputs			0.5	mA
<b>Input CSB</b>						
Input voltage low					0.3	VIO
Input voltage high			0.7			VIO
Hysteresis (note 1)		VCC = 8.5V	0.1			V
Leakage current		Pin at VIO	-1		1	µA
Pull-up resistance			125		750	kOhm
<b>Input SCLK</b>						
Input voltage low					0.3	VIO
Input voltage high			0.7			VIO
Hysteresis (note 1)		VCC = 8.5V	0.1			V
Leakage current		Pin at VSS	-1		1	µA
Pull-down resistance			125		750	kOhm
<b>Input SI</b>						
Input voltage low					0.3	VIO
Input voltage high			0.7			VIO
Hysteresis (note 1)		VCC = 8.5V	0.1			V
Leakage current		Pin at VIO or VSS	-1		1	µA

Output SO						
Output voltage low		$I_{out} < 500 \mu A$			0.2	VIO
Output voltage high		$I_{out} > -500 \mu A$	0.8			VIO
Leakage current when in tri-state		Pin at VIO or VSS	-10		10	$\mu A$
Output ERRB						
Output voltage low		$I_{out} < 500 \mu A$			0.3	V
High level output leakage current		pin at VIO			10	$\mu A$
Output SIN1P, SIN1M, COS1P, COS1M, SIN2P, SIN2M, COS2P, COS2M						
Drop-out voltage for each pair of buffers		VCC=8.5V, Tamb=25degC, I=30mA			1.6	V
Mismatch of drop-out voltage		VCC=8.5V, Tamb=25degC, I=30mA	-50		50	mV
Output OUT3						
Output voltage low		VCC=8.5V, Tamb=25degC, I=40mA			0.6	V
Output voltage high		VCC=8.5V, Tamb=25degC, I=-40mA	6.8			V

Table 6: Static electrical specifications

Note:

1. Not tested in production, guaranteed by design.
2. The voltage at VIO should never exceed the voltage at VCC.

## 10.2 Dynamic characteristics

Table 7 shows the dynamic characteristics of the chip. DC Operating Parameters are default  $T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ ,  $V_{\text{sup}} = 4.5\text{V}$  to  $12\text{V}$ , unless otherwise specified.

Parameter.	Symbol	Test Conditions	Min	Typ	Max	Units
<b>On chip oscillator</b>						
Clock frequency	Fclku	At $V_{\text{sup}} = 12\text{V}$ , uncalibrated	0.7	1	1.7	MHz
Absolute tolerance of the clock frequency after calibration	Tolclka	At $V_{\text{sup}} = 12\text{V}$ , $25^{\circ}\text{C}$ , after full calibration to 1MHz	-10		10	%
Temperature variation of the clock frequency after calibration	Tolclkt	At $V_{\text{sup}} = 12\text{V}$ , after full calibration to 1MHz	-6		6	%
<b>Serial communication</b>						
Recommended Frequency of SPI Operation	FSPI			0.5	1.0	MHz
Falling edge of CSB to Rising Edge of SCLK (Required Setup Time) (note 7)	TLEAD		20			ns
Falling edge of SCLK to Rising Edge of CSB (Required Setup Time) (note 7)	TLAG		20			ns
SI to Falling Edge of SCLK (Required Setup Time) (note 7)	TSISU		75			ns
Falling Edge of SCLK to SI (Required Hold Time) (note 7)	TSI		75			ns
SO Rise Time ( $CL=200\text{pF}$ ) (note 7)	TRSO				75	ns
SO Fall Time ( $CL=200\text{pF}$ ) (note 7)	TFSO				75	ns
SI, CSB, SCLK, Incoming Signal Rise Time (Note 1, 7)	TRSI				75	ns
CSB, SCLK, Incoming Signal Fall Time (Note 1, 7)	TFSI				75	ns
Rising Edge of CSB to Falling Edge of CSB (Required Setup Time) (Note 5, 7)	TCSB		32			$\mu\text{s}$

Rising Edge of VCC to Falling Edge of CSB (Required Setup Time) (Note 6, 7)	TEN		10		ms
Time from Falling Edge of CSB to SO Low Impedance (Note 2, 7)	TSO_EN			150	ns
Time from Rising Edge of CSB to SO High Impedance (Note 3, 7)	TSO_DIS			150	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 4, 7) 0.2 VCC <= SO > = 0.8 VCC, CL = 200 pF	TVALID			150	ns

Table 7: Dynamic characteristics MLX10420

Note:

1. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
2. Time required for output status data to be available for use at SO. 1 K Ohm load on SO.
3. Time required for output status data to be terminated at SO. 1 K Ohm load on SO.
4. Time required to obtain valid data out from SO following the rise of SCLK.
5. This value is for a 1 MHz calibrated internal clock; it will change proportionally as the internal clock frequency changes.  
Writing to register AIRCORE1 and AIRCORE2 need special attention. Consecutive writing to one of these registers must have a delay of at least 256usec (with 1MHz on-chip oscillator). For more information see 11.6.1.
6. The SPI interface can be used only after chip self-test (about 10mS at 1 MHz calibrated internal clock).
7. This parameter is 'guaranteed by design', and not measured during production.

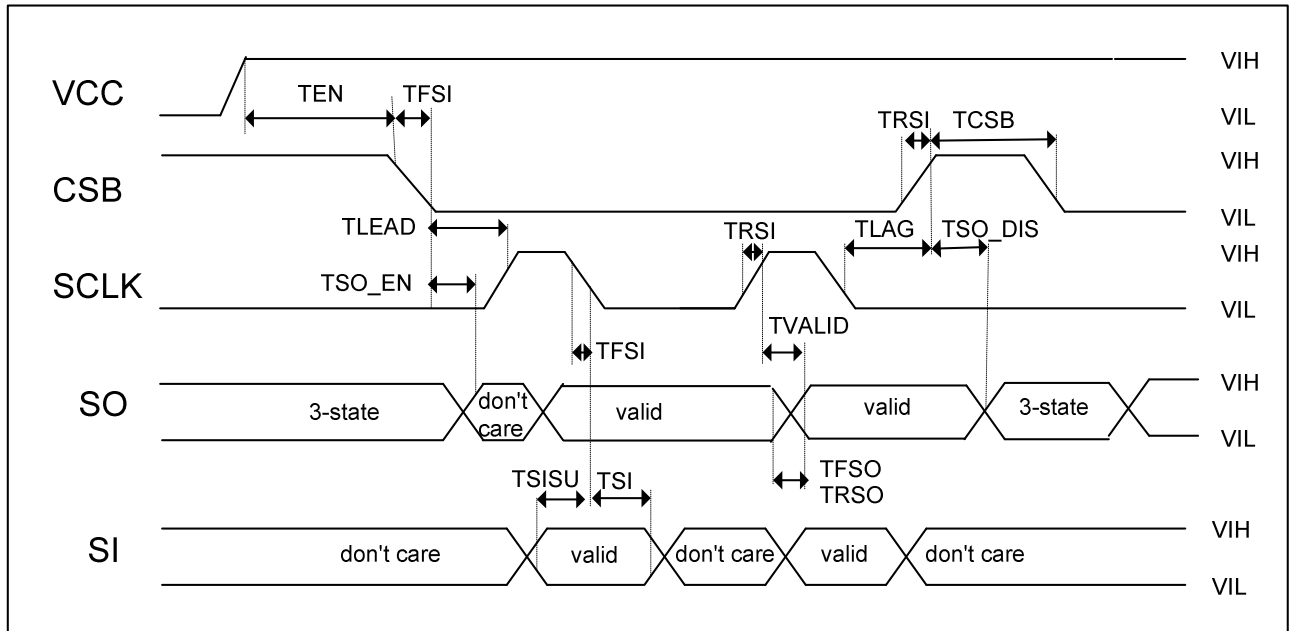


Figure 2: SPI timing characteristics

## 11 Detailed block diagram description

### 11.1 Block diagram digital part

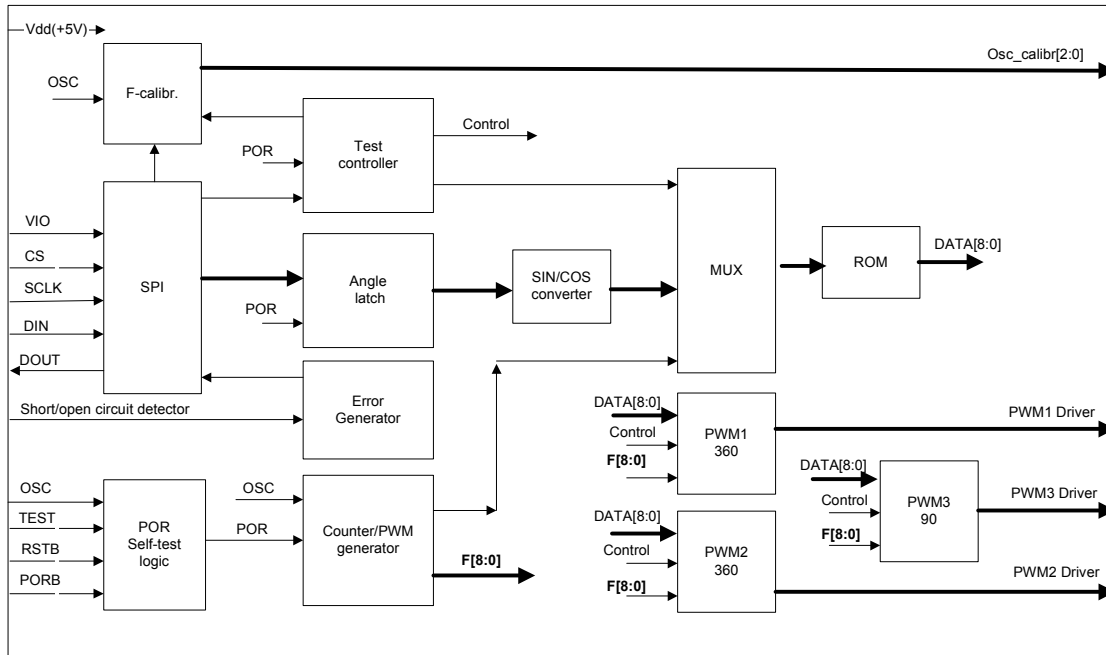


Figure 3: Digital part block diagram

### 11.2 Gauge driver operation

#### 11.2.1 Air-core meters 360°

Immediately after a reset, the chip checks if there is any short-circuit or open circuit on each buffer driver output (This test is not made for output OUT3). For this test, each buffer is held in a high impedance state and large internal resistances (100kΩ) are sequentially connected on each pair of buffers (note : the actuator coil must be connected on each bridge).

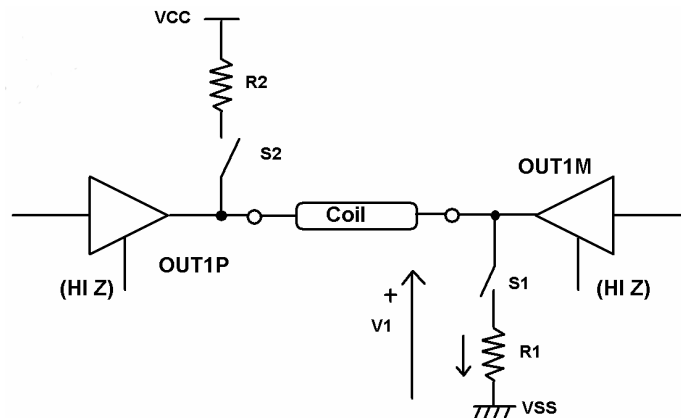


Figure 4: Test for short-circuits and open circuits

Three tests are done (see Figure 4):

	condition	test for :
Test 1	S1 closed, S2 open	V1 = VSS
Test 2	S1 closed, S2 closed	V1 = VCC/2
Test 3	S1 open, S2 closed	V1 = VCC

Table 8: Self test description

During the tests the pin ERRB is at logic level 0. When the tests are finished ERRB stays at 0 if one (or more) test fails or changes to high impedance state if everything is OK.

These tests last approximately 6 ms.

After the test all buffers are at VSS. The chip waits for the  $\mu\text{P}$  to send an angle/quadrant value and then outputs a PWM signal on every buffer. Every air-core meter coil is connected in a bridge, so the current  $I_{\text{coil}}$  can be either positive or negative. The total drop-out of a bridge is:

$$V_d = |V_{CC} - V_{\text{coil}}|$$

The four bridges have the same drop-out for the same current  $I_{\text{coil}}$ .

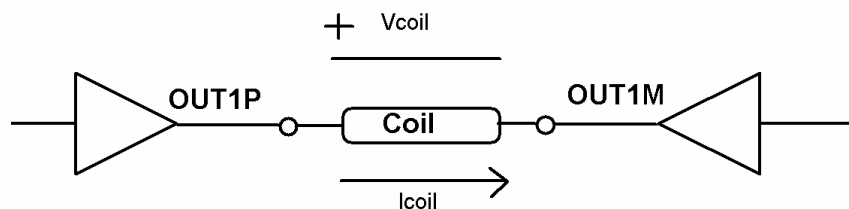


Figure 5: Full bridge configuration

### 11.2.2 air-core meter 90°

There is one PWM output for air-core meter 3. During reset the driver is put at VCC.

## 11.3 Angle tracking

The generation of the angle for the air-core meters 1 and 2 (the 360° air-core meters) consists of an angle value and a quadrant definition. The chip continuously monitors that the angle values received are consistent. If there is no continuity between two consecutive quadrant values sent (for AIRCORE1 or AIRCORE2) an error is generated and the last received angle value is discarded. The previous values are kept and the  $\mu$ P must initialize a new transmission to the chip. The error can be read via the ERRB output (see par. 11.5) or via the status register (see par. 11.4.6).

If an angle value is sent to the chip with the control bit AT set to '0', then the angle tracking is disabled and the new angle value will always be accepted.

## 11.4 Serial link

### 11.4.1 Introduction

The SPI interface has a full duplex, three-wire synchronous, 16-bit serial synchronous interface data transfer and four I/O lines associated with it: SI, SO, SCLK, and CSB. The SI/SO pins follow a first in / first out (D0 / D15) protocol with both input and output words transferring the least significant bit first.

The I/O pins are supplied via the pin VIO. By connecting this pin VIO to the supply of the  $\mu$ P interface pins a perfect interface is guaranteed for all types of  $\mu$ P.

### 11.4.2 Signal description

The Chip Select (CSB) pin enables communication with the master device. When this pin is in a logic [0] state, the chip is capable of transferring information to, and receiving information from, the master. The chip latches data in from the Input Shift registers to the addressed registers on the rising edge of CSB. The output driver on the SO pin is enabled when CSB is logic [0]. When CSB is logic high, signals at the SCLK and SI pins are ignored; the SO pin is tri-stated (high impedance). CSB will only be transitioned from a logic [1] state to a logic [0] state when SCLK is a logic [0]. CSB has an internal pull-up connected to the pin.

SCLK clocks the Internal Shift registers of the chip. The Serial Input (SI) pin accepts data into the Input Shift register on the falling edge of the SCLK signal while the Serial Output pin (SO) shifts data information out of the SO Line Driver on the rising edge of the SCLK signal. It is important the SCLK pin be in a logic [0] state whenever the CSB makes any transition. SCLK has an internal pull down. When CSB is logic [1], signals at the SCLK and SI pins are ignored; SO is tri-stated (high impedance). See the Data Transfer Timing diagrams in Figure 6 and Figure 7.

The SI pin is the input of the Serial Peripheral Interface (SPI). Serial Input (SI) information is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, beginning with the least significant bit (LSB). After transmitting a 16-bit word, the CSB pin has to make a transition to a logic [1] before transmitting a new word. SI information is ignored when CSB is in a logic high state.

The Serial Output (SO) data pin is a tri-stateable output from the Shift register. The Status register bits will be the first 16-bits shifted out. Those bits are followed by the message bits clocked in FIFO, when the device is in a daisy chain connection, or being sent words of 16-bit multiples. Data is shifted on the rising edge of the SCLK signal. The SO pin will remain in a high impedance state when the CSB pin is put into a logic high state.

### 11.4.3 Functional description

This section provides a description of the chip SPI behaviour. To follow the explanations below, please refer to the timing diagrams shown in Figure 6 and Figure 7.

Pin	Description
CSB (1 to 0)	SO pin is enabled
CSB (0 to 1)	The chip configuration and desired output states are transferred and executed according to the data in the shift registers.
SO	Will change state on the rising edge of the SCLK pin signal
SI	Will accept data on the falling edge of the SCLK pin signal

Table 9: Data transfer timing

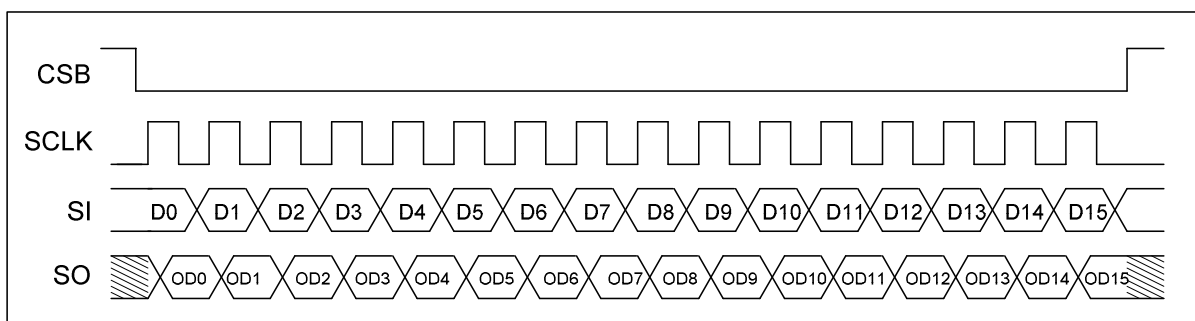


Figure 6: Single 16-bit word SPI communication timing diagram

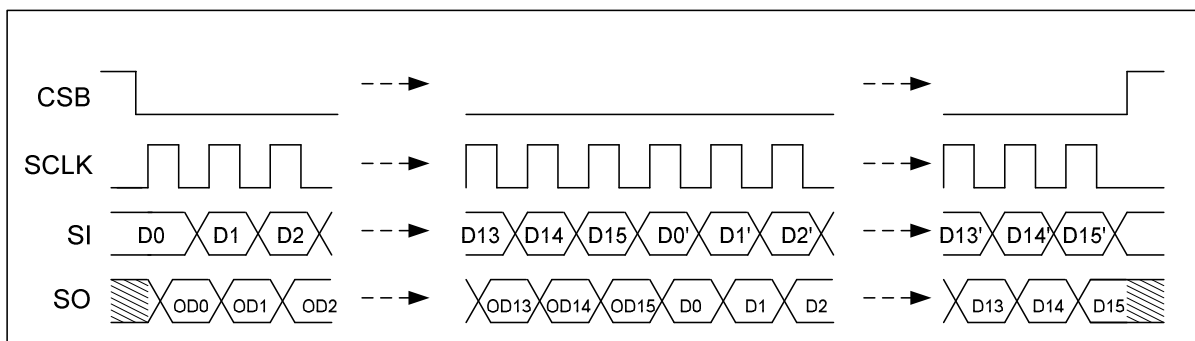


Figure 7: multiple 16-bit word SPI communication timing diagram

#### DATA INPUT

The input Shift register captures data at the falling edge of the SCLK clock. The SCLK clock pulses exactly 16 times only inside the transmission windows (CSB in a logic [0] state). By the time the CSB signal goes to logic [1] again, the contents of the Input Shift register are transferred to the appropriate internal register, according to the address contained in bits 1-3. The signal CSB should be kept high for a minimum time as defined in Table 7. That data is specified in Figure 2. It must be long enough so that the internal clock is able to capture the data from the input Shift register and transfer it to the internal registers.

#### DATA OUTPUT

At the first rising edge of the SCLK clock, with the CSB at logic [0], the contents of the Status Word register are transferred to the Output Shift register. The first 16 bits clocked out are the status bits. If data continues to

clock in before the CSB transitions to a logic [1], the device to shift out the data previously clocked in FIFO after the CSB first transitioned to logic [0].

### 11.4.4 Communication memory maps

The chip is capable of interfacing directly with a micro controller, via the 16-bit SPI protocol described and specified below. The device is controlled by the microprocessor and reports back status information via the SPI. This section provides a detailed description of all registers accessible via serial interface. The various registers control the behaviour of this device.

A message is transmitted by the master beginning with the LSB (D0) and ending with the MSB (D15). Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Data is transferred through daisy chained devices, illustrated in Figure 7.

The chip uses seven registers to configure the device and control the state of the outputs. The registers are addressed via D1-D3 of the incoming SPI word, as described in Table 10.

Address [D3:D1]	Use	Name
001	Writing request air-core 1	AIRCORE1
011	Writing request air-core 2	AIRCORE2
100	Writing request air-core 3	AIRCORE3
101	Chip reset	RST
110	Oscillator calibration	CAL
111, 010, 000	test	TST

Table 10: Memory map

Writing to the test addresses will have no effect in normal operation mode, i.e. when input TEST is at VSS.

On the low to high transition of CSB the values in the receiver buffer are stored into the internal registers of the chip if no angle tracking error was detected by the chip.

The chip outputs an error status on pin ERRB within 2usec after the rising edge of CSB. The output ERRB goes back to tri-state at the next rising edge of CSB if no new angle tracking error is detected, or after chip reset.. The error status can also read via the status register.

### 11.4.5 Register description

#### 11.4.5.1 AIRCORE1

Address: 001																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<b>write</b>	x	P11	P12	P13	P14	P15	P16	P17	P18	P19	Q10	Q11	0	0	1	AT

These bits are write-only.

- P10 – P19: value of the requested angle, P11 is LSB.
- Q10 – Q11: value of the requested quadrant.
- AT: angle tracking is switched on if set to '1', switched off if set to '0'.

## 11.4.5.2 AIRCORE2

Address: 011																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<b>write</b>	x	P21	P22	P23	P24	P25	P26	P27	P28	P29	Q20	Q21	0	1	1	AT

These bits are write-only.

- P21 – P29: value of the requested angle.
- Q20 – Q21: value of the requested quadrant.
- AT: angle tracking is switched on if set to '1', switched off if set to '0'.

## 11.4.5.3 AIRCORE3

Address: 100																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<b>write</b>	x	P31	P32	P33	P34	P35	P36	P37	P38	P39	x	x	1	0	0	x

These bits are write-only.

- P31 – P39: value of the requested angle, P31 is LSB

## 11.4.5.4 CAL

Address: 110																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<b>write</b>	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0	x

These bits are write-only.

Bits D0 and [D4:D15] are 'don't care'.

Principle of operation:

- The osc has 4 bits of trimming TRIM[3:0].
- After reset the oscillator starts at typical frequency (TRIM[3:0] = 1000).
- When the chip receives a CAL command it enters a special calibration mode.
  - The oscillator is put to minimum frequency, i.e. TRIM[3:0] is reset to 0000.
  - The uP will send pulses on the CSB line of 17.5 usec. During these pulses the SCLK line must remain low. (Time between two consecutive pulses must be 10 usec minimum).
  - During each of these pulses the chip counts a 4 bit counter to check its frequency.
  - If the on chip frequency is too low it will increase its trimming state with 1.
  - The uP can send as many pulses as he wants. After max 16 pulses the chip has its optimal frequency.
  - The chip leaves this mode as soon as a transition on SCLK is detected. This can be the first rising edge of SCLK in a normal SPI communication.
  - During the calibration mode the output SO remains in tri-state.
- During CAL, the drivers can be active, but can not change state.
- If the uP applies pulses longer or shorter than 17.5usec, the oscillator can be calibrated to an other frequency (within its trimming range).

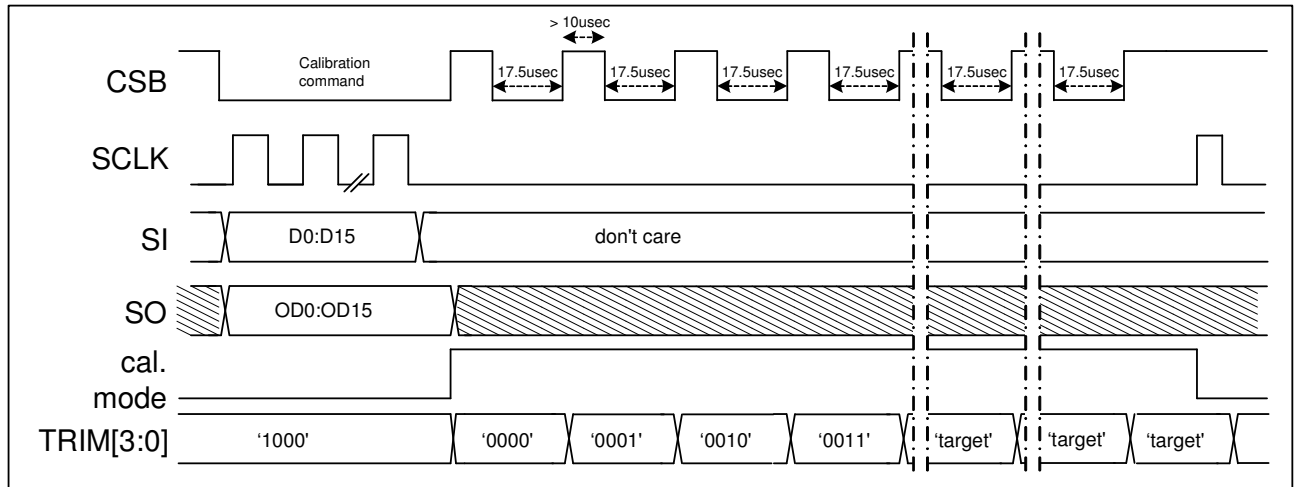


Figure 8: Calibration sequence timing diagram

### 11.4.5.5 RST

Address: 101																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
write	x	x	x	x	x	x	x	x	x	x	x	x	1	0	1	x

These bits are write-only.

All bits are 'don't care'.

When writing to this address, the chip will initiate an on-chip reset pulse when CSB goes high. The reset signal will be active for one period of the on-chip oscillator. After that the normal startup sequence is started.

### 11.4.5.6 TEST

Any other codes are reserved for test. Users are not allowed to use these modes.

### 11.4.6 Status register

Status																
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
read	0	0	0	0	0	0	0	0	0	0	0	0	EAT	EL2	EL1	x

These bits are read-only.

- EAT: angle tracking error. This bit is read as '1' if an angle tracking error was detected during the previous message.
- EL1: load error for driver AIRCORE1. This bit is set to '1' if an error is detected during the self test procedure after reset.
- EL2: load error for driver AIRCORE2. This bit is set to '1' if an error is detected during the self test procedure after reset.
- EAT: angle tracking. This bit is read as '1' if an angle tracking error was detected for AIRCORE1 or AIRCORE2 during the previous message.

Transmission of the status register is done beginning with the LSB (D0) and ending with the MSB (D15).

### 11.5 Error output

The chip has an error output ERRB. This is a pull down output driver. It is active low when indicating an error, and tri-state when no error is indicated.

There are 3 possible indications:

- The chip is in reset – self test mode.
- Detection of error during the self test procedure following the reset (see par. 1411.2.1). In this case the ERRB output remains low. It can only go to tri-state by restarting the self test procedure.
- Detection of an angle tracking error (if enabled). The chip outputs this error status within 2usec after the rising edge of CSB. The output ERRB goes back to tri-state at the next rising edge of CSB if no new angle tracking error is detected, or after chip reset.

### 11.6 PWM generation

#### 11.6.1 Air-core meter 360°

From the angle value received from the  $\mu$ P (range  $[0^\circ - 89.8^\circ]$ ) the chip generates two PWM signals with 9 bits resolution:

- the first one represents the sine PWMSIN
- the second one is the cosine PWMCOS

The chip uses a ROM 512x9 which contains the sine of any angle in the range  $[0^\circ - 89.8^\circ]$  (note that the LSB value of the angle is not used).

A value of angle greater than  $90^\circ$  is obtained using different quadrant values:

quadrant	D4:D5	angle
Q1	00	$0^\circ \leq \alpha < 90^\circ$
Q2	01	$90^\circ \leq \alpha < 180^\circ$
Q3	10	$180^\circ \leq \alpha < 270^\circ$
Q4	11	$270^\circ \leq \alpha < 360^\circ$

Table 11: Quadrant definition

The PWM signals are switched to the outputs depending on the value of the quadrant:

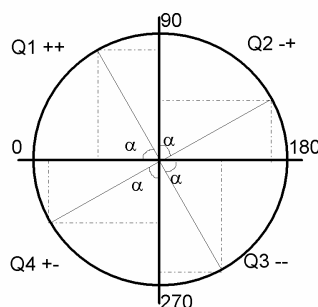


Figure 9: Quadrants and PWM sign

quadrant	angle	D4:D5	SIN1M	SIN1P	COS1M	COS1P
Q1	$0^\circ \leq \alpha < 90^\circ$	00	0	PWMSIN	0	PWMCOS
Q2	$90^\circ \leq \alpha < 180^\circ$	01	0	PWMCOS	PWMSIN	0
Q3	$180^\circ \leq \alpha < 270^\circ$	10	PWMSIN	0	PWMCOS	0
Q4	$270^\circ \leq \alpha < 360^\circ$	11	PWMCOS	0	0	PWMSIN
Reset = Q1	0	00	0	0	0	0

Table 12: PWM definition

air-core meter 1 is driven by outputs SIN1M/P and COS1M/P.  
air-core meter 2 is driven by outputs SIN2M/P and COS2M/P.

The PWM frequency is given by  $FPWM = FOSC / 512$  where FOSC is the frequency of the on chip oscillator.

When the chip receives an SPI command that writes to AIRCORE1 or AIRCORE2, the received angle is transferred to an intermediate latch at the rising edge of CSB. After that moment the received angle is verified (if the angle tracking feature is enabled) within 32 usec. If accepted, the angle is transferred to the corresponding PWM generator circuit at the start of the next PWM period. The delay between reception of the SPI command and the transfer to the output will be not more than 256usecs typically. If the uP sends a next SPI command to the same register before the previous data were sent to the PWM generator, the previous data will be lost and overwritten by the new received angle. The risk exists that the air-core gauge meter receives data from different, non-adjacent quadrants.

After reset the 4 outputs go to 0, meaning the angle is 0.

### 11.6.2 Air-core meter 90°

The value in bits D6:D14, transmitted by the  $\mu P$ , is directly the PWM value. D0, D15 and the quadrant bits D4:D5 are not used. A PWM of 0% corresponds to an output constantly at VCC, a PWM of 100% corresponds to an output constantly at VSS.

When the chip receives an SPI command that writes to AIRCORE3, the received angle is transferred to an intermediate latch at the rising edge of CSB. The angle is transferred to the corresponding PWM generator circuit at the start of the next PWM period. The delay between reception of the SPI command and the transfer to the output will be not more than 256usecs typically. If the uP sends a next SPI command to the same register before the previous data were sent to the PWM generator, the previous data will be lost and overwritten by the new received angle.

After reset the PWM is set to 0%, meaning the output goes to VCC.

### 11.7 Test

For efficient testing of the chip a test input pin TEST is foreseen. This pin must be connected to VSS during normal operation.

## 12 Applications Information

Following is an example of an application diagram with 2 360° air-core meters and 1 90° air-core meter.

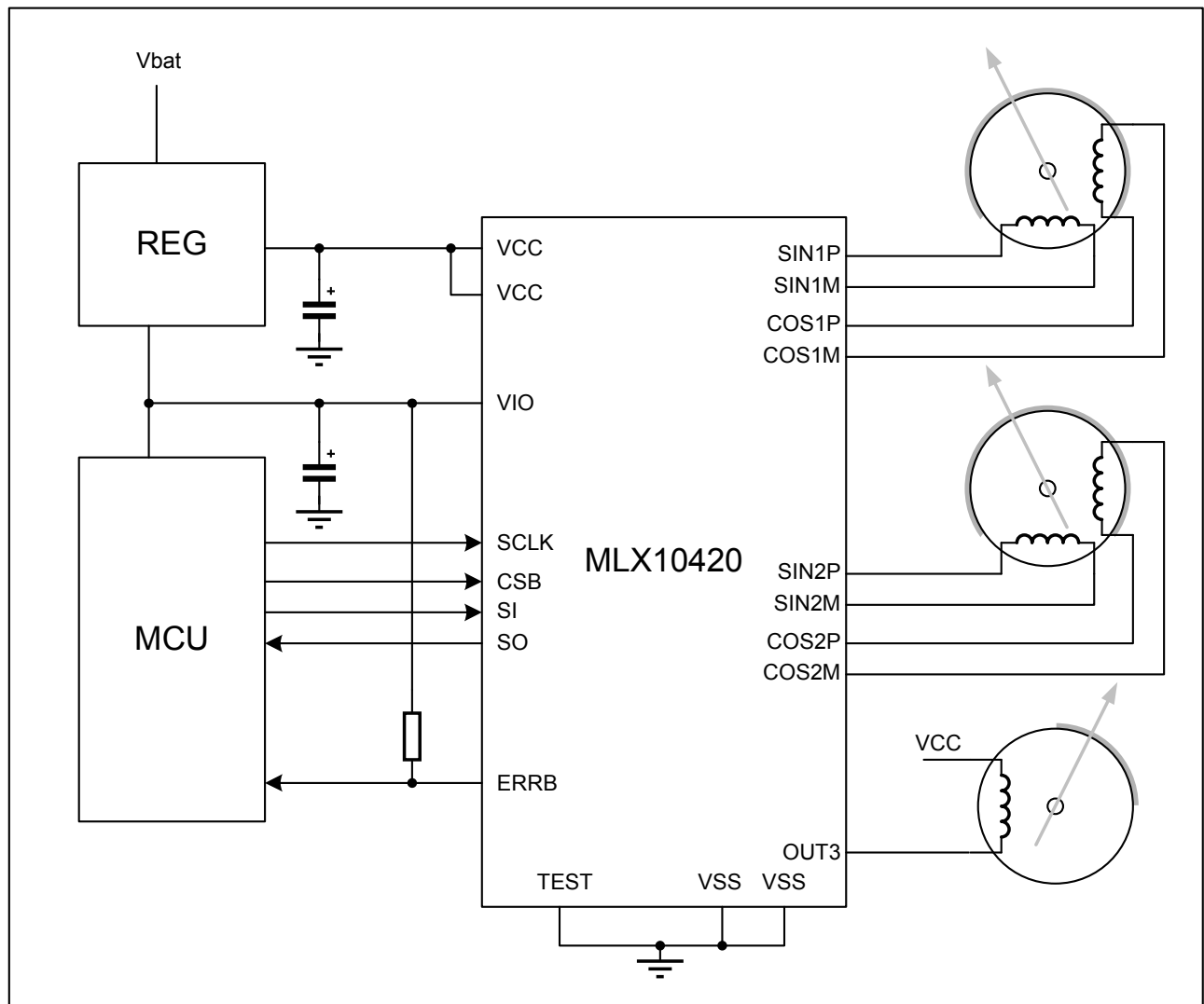


Figure 10: Typical application diagram

## **13 Reliability Information**

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

### **Reflow Soldering SMD's (Surface Mount Devices)**

- IPC/JEDEC J-STD-020  
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices  
(classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113  
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing  
(reflow profiles according to table 2)

### **Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)**

- EN60749-20  
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat

### **Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)**

- EIA/JEDEC JESD22-B102 and EN60749-21  
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMDs is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a Roadmap to qualify their package families for lead free processes also.  
Various lead free generic qualifications are running, current results on request.

For more information on manufacturability/solderability see quality page at our website:  
<http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf>

## **14 ESD Precautions**

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).  
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

## 15 Package Information

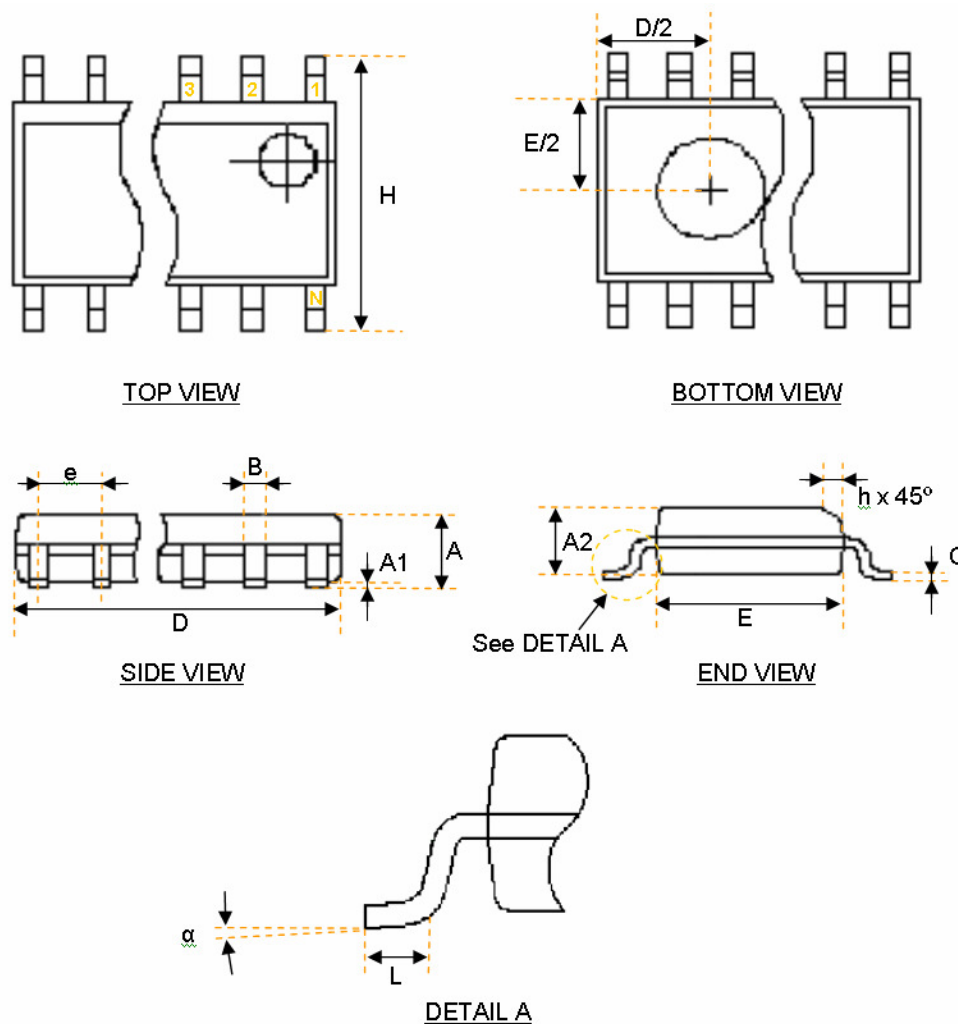


Figure 11: Package information drawing

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
B	0.25		0.38
C	0.09		0.20
D	7.07	7.20	7.33
E	5.20	5.30	5.38
e		0.65	
H	7.65	7.80	7.90
L	0.63	0.75	0.95
N		20	
α	0°	4°	8°